Design of a 8 Watt, High efficiency X-band Power PHEMT Amplifier

Agilent EEsof EDA

Innovative Solutions, Breakthrough Results
ADS MMIC Layout Tool Bar: UMS PPH25X

Layout editing commands are easily accessible and are configured to work seamlessly with the UMS foundry process.
Single-button for Design & Verification

Layout editing:
• convert traces to transmission-line elements
• edit transmission-line elements (stretch, tap, split, move to layer)
• automatically insert vias
• automatically create multi-layer metal traces
• synchronize layout back to the schematic

Verification:
• Check design differences between layout & schematic
• Launch 3D Layout Viewer
• Launch ADS Desktop DRC & LVS
• Automatically generate a reticle
• Show nodal and physical connectivity
3D Layout Viewer

Validate layer connectivity using “Cut Plane” cross-section view in the 3D Viewer
ADS Desktop DRC for UMS PPH25X

- Included in the New Layout
- No license denials
- No waiting for results
- IP never leaves your desktop
- Highlights errors in the layout
- Zooms to X & Y co-ordinates
- Browser groups & filters errors
- Supports device recognition
- And much more …
ADS Desktop LVS

• Catch errors early by running ADS Desktop LVS from within ADS schematic or layout
• No Rules File Needed
Reticle Generation
Package Assembly Tool

Combining multiple technologies for 3D EM simulation
Agilent EEsof Integrated 3D EM Flow

EMPro link with ADS

Package Design

EMPro Platform

Parameterized 3D Components

Layout CAD Data

MMIC Design

ADS Platform

FDTD Simulator

FEM Simulator

Momentum Simulator
Complete MMIC ADS Desktop Design Flow

- Models & Enhanced Foundry Kits
- ADS Desktop DRC / Calibre / Assura / mailDRC
- 3D Planar EM Design & Verification
- ADS Desktop LVS / Calibre
- Mask Reticle
- Packaging & Module
- Integrated 3D EM Analysis and Design

- Design for Mfg
- Schematic/Circuit Design & Tools
- Physical Design & Layout
- Hardware Validation/Connected Solutions
- DUT Board

- Optimization, Yield & Statistical Design
- X-Parameters Non-linear Behavioral Modeling
- ADS Ptolemy Performance Verification

Agilent Technologies
Design of a 8 Watt, High efficiency X-band Power PHEMT Amplifier

T. Huet, C. Byl, V. Serru

Presented by

Emilee Elliott (1), Joe Civello (1), Jack Sifri (1), Belinda Piernas (2), Philippe Labasse (2), Thibaut Huet (2)

March 16th, 2010

(1) Agilent
(2) United Monolithic Semiconductor is a company of THALES and EADS
Outline

- Company profile
- Motivation
- Considerations on HPA
  - Transistors characterization
- UMS PPH25X technology
  - Harmonic Balanced Simulations (standard + 3D planar)
  - Measurements
  - Main performances and layout
- Design methodology
- 2-stage HPA
- Conclusion
- ADS AGILENT software & UMS design kits
Company profile: UMS Main Market Segments

**Defence & Security**
- Phased Array Radar (PAR)
- Electronic Warfare (EW)
- Security Sensors

**Space**
- Communication Satellite
- Earth Observation
- Phased Array Radar

**Automotive / ISM**
- LRR 77GHz
- SRR 24/79GHz
- Tolling
- Industrial Sensors

**Telecom**
- Point to Point
- Point to Multi-Point
- VSAT
- BTS
## Company profile: UMS technology Roadmap

<table>
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</tbody>
</table>

**Research**
- Research & Development
- Industrialization and Qualification
- Production
- Space Evaluation
- Space Evaluated
Company profile: UMS Sales Network

UMS USA, Inc.
- Lowell, MA – USA
- Customer Support and Design Center

UMS SAS - EUROPE
- Orsay – France
- Design & Manufacturing

UMS GmbH
- ULM - Germany
- Manufacturing

THALES Italia
- ROMA – Italy
- Sales Office

UMS - ASIA
- Shanghai - PR China
- Sales Office

WW Distribution
- And Regional Representatives network
Motivation

Monolithic Microwave Integrated Circuits HPAs based on Gallium Arsenide are dedicated to T/R modules for Phased Array radars. Very high efficiency and high power are required for these X band applications without linearity constraints.

The design goal was to demonstrate that the UMS Power PHEMT technology (PPH25X) enables the generation of powerful and robust HPAs using the “Advanced Design System” software from Agilent for electromagnetic simulations.
UMS PPH25X Technology

MAIN FEATURES

- Space evaluated technology (ESA)
- Double recess 0.25 µm gate length
- High power density (0.85W/mm) @10 GHz, with Vd=8V
- High gain (16dB at 10 GHz for power cell 12X130µm)
- High breakdown voltage (Vbds ~ 20 V)
- Over vias MIM Capacitors
- 70 µm substrate thickness with small via-holes
Transistors Characterization

- In order to reach good performances at HPA level, a good knowledge of the transistors is required.

- Transistors accuracy is based on standard measurements:
  - S parameters measurements:
  - Pulsed I-V measurements:
  - Load pull measurements:

  - To define transistor optimum loads for output power, PAE and drain current.
Design methodology

- **Class A-B amplifier**

- **Choose the transistor size and optimum load impedance taking into account:**
  - Linear gain, Pout, PAE
  - Frequency band
  - Output mismatch (VSWR=2:1)
  - Safe operating area (robustness)

- **HPA matching network (output combiner,...)**

- **Non linear stability analysis (odd and even mode)**
ADS Tools for HPA designs

- **Load pull simulations**

- **Optimization/Tuning for matching network generation**

- **“Standard” simulations**
  - Small signal simulations (S parameters)
  - Harmonic balanced simulations (non-linear simulations)
  - Time domain simulations (switching time specifications)

- **EM simulations for passive networks**: Momentum simulations to check coupling effects, symmetries and proximities.

- **Statistics:**
  - Technological spread analysis to check design sensitivity and give expected electrical yields

- **Auto-layout generation and Design Rules Checker**
Transistors selection: Loadpull by simulation

Specify desired Fundamental Load Tuner coverage:

- \( s_{11} \text{_rho} \) is the radius of the circle of reflection coefficients generated. However, the radius of the circle will be reduced if it would otherwise go outside the Smith Chart.
- \( s_{11} \text{_center} \) is the center of the circle of generated reflection coefficients.
- \( p \) is the total number of reflection coefficients generated.
- \( Z_{0} \) is the system reference impedance.

- \( \text{VAR} \) Sweep Equations:
  - \( e_{1} = \text{_s11} \)
  - \( \text{_center} = 0.44 \) (0.15^
  - \( p = 400 \)
  - \( Z_{0} = 50 \)

\( s_{11} \text{_rho} \) is the radius and \( s_{11} \text{_center} \) is the center of the circle. (But this is just a static drawing.)

Refer to the data display file "ReflectionCoeffUtility" for help in setting \( s_{11} \text{_rho} \) and \( s_{11} \text{_center} \). Also refer to the example design file, exampleRF_Board_LoadingProfile_FundamentalLoadPull_4 enter "LoadPull" for details about how this simulation is run.

One Tone Load Pull Simulation:
Output power and PAE found at each fundamental load impedance.

Ref: AGILENT / UMS Webinar
date: March 2010
Transistors selection: Loadpull by simulation

Load pull for PAE contours

Good accordance between Measurements and simulation

Load pull Measurements on PPH25X transistor

Simulation with ADS software using UMS transistor model

Transistor size: 12 x 130 µm
Frequency = 10 GHz
Vgs=-0.35V, Vds=8V

PAE Contours

m1
indep(m1)=1
PAE contours p=0.684 / 148.997
level=60.974116, number=1
impedance = 10.089 + j13.342

PAE step 5 %
2-stage HPA: Specifications

The HPA was developed in the frequency Band: 8.5-11.5 GHz.

- **2-STAGE VERSION**

  Design goal @25°C: Pout>8W, PAE>35%, Linear Gain= 20 dB

  Pulse conditions for drain: 25µs, 10%

  No specifications on linearity

  Chosen topology:

  First stage: 2 power cells (12x130 µm)
  Second stage: 8 power cells (12x130 µm)
2-stage HPA: Output Combiner optimization

Combiner optimisation

8-12GHz: Low insertion losses

UMS passive components
from dk PPH25X

Agilent microstrip models
2-stage HPA: Output Combiner checking

Combiner symmetry

8.5-11.5GHz

Low insertion losses

Agilent 3D planar momentum
2-stage HPA: Output Combiner 3D View
2-stage HPA: simulation with ADS software
2-stage HPA: simulation with ADS components

Monte Carlo analysis: 150 iterations in order to check HPA linear performances versus technological spread
2-stage HPA: simulation with ADS software

ADS components from UMS PPH25X design Kit and ADS libraries

ADS components from UMS PPH25X design Kit and ADS libraries + 3D planar momentum Simulation
2-stage HPA: simulation with ADS software

3D planar momentum Simulation for Passive Networks:
SUBSTRATE DEFINITION FOR PPH25X TECHNOLOGY
By using PPH25X Design Manual
2-stage HPA: Non Linear Stability analysis (*)

**Stability**

Wide band stability checking vs Frequency band, Input power and odd and even modes

Instability occurred when:
Real(Zp) ≤ 0 AND Imag(Zp) = 0
with Imag(Zp) crossing the zero from negative values to positive values.

(*) developed by Bilbao University (Spain)
2-stage HPA: simulation with ADS software

Linear Gain and compressed gain @3dB compression vs frequency @20°C

Drain voltage = 8V
Quiescent current = 2A
2-stage HPA: measurements

Linear Gain vs Temperature

Pulsed drain measurements: 8V
Quiescent current = 2A
Pulse width = 100µs
Duty cycle = 30%

![Graph showing linear gain vs frequency at different temperatures](image_url)
2-stage HPA: simulation with ADS software

Output Power for 3dB comp. vs Pin

Drain measurements: 8V
Quiescent current= 2A
2-stage HPA: measurements

Output Power for 3dB comp. vs Pin

Pulsed drain measurements: 8V
Quiescent current = 2A
Pulse width = 100µs
Duty cycle = 30%

![Graph showing output power vs frequency](image-url)
2-stage HPA: simulation with ADS software

PAE for 3dB comp. vs frequency
@+20°C

Drain voltage = 8V
Quiescent current = 2A

Drain voltage= 8V
Quiescent current= 2A
2-stage HPA: measurements

PAE for 3dB comp. vs Pin

Pulsed drain measurements: 8V
Quiescent current= 2A
Pulse width= 100µs
Duty cycle= 30%

Power added efficiency (%) vs Frequency (GHz)
2-stage HPA: simulation with ADS software

Id for 3dB comp. vs frequency
@+20°C

Drain voltage= 8V
Quiescent current= 2A
2-stage HPA: measurements

Id for 3dB comp. vs Pin

Pulsed drain measurements: 8V
Quiescent current = 2A
Pulse width = 100µs
Duty cycle = 30%

![Graph showing drain current vs frequency](image-url)
2-stage HPA: measurements

Output power @20°C vs compression

Pulsed drain measurements: 8V
Quiescent current= 2A
Pulse width= 25µs
Duty cycle= 10%

PAE @20°C vs compression

Robustness test vs overdrive
2-stage HPA: measurements

Robustness test in worst cases

**Conditions:**
- Bandwidth: 8.5-11.5 GHz
- Drain voltage 8V
- VSWR 2:1
- 8 Phase states
- Short Pulses
- -40°C
- 6dB gain compression

No degradation after stress test

Output power vs phase state

Frequency = 10 GHz
2-stage HPA: main performances

**Performances**
- 8.5-11.5 GHz
- Small signal gain 19-20dB
- Sat. output power: >8W
- Sat. PAE: > 40%

**Thermal aspect**
- Channel temperature < 165°C
- with backside temperature of +80°C

**Features**
- DC Power consumption: 18.4W
- Chip size: 4.41x 3.31x 0.07mm
- Chip area: 14.6 mm²

**Reliability**
- RF life test exhibits no degradation of the device after 2000 hours at +70°C in CW mode@ 5 dB compression
Summary of difficulties faced during the design

- Symmetry of 2\textsuperscript{nd} stage transistors loads generated by the output combiner
- Inter-stage optimization: compromise between losses and impedance generation for the first stage versus frequency.
- Non linear stability analysis versus odd and even modes:
  (worst case on 2\textsuperscript{nd} stage: 8 transistors)
Conclusion

- Today during this webcast, the development of robust HPAs with high level of PAE and high output power has been presented on about 30% of frequency Band thanks to “Advanced Design System” from AGILENT.

- This device is available as a catalog product: CHA7114. Based on the good accuracy between simulation and measurements, a new portfolio of HPA has been developed:
  
  - C Band, Pout >12 W, PAE > 40%, Gain=24 dB: not yet a product
  - X Band, Pout >9 W, PAE=35%, Gain=28 dB: CHA7215
Foundry Partners - United Monolithic Semiconductors

United Monolithic Semiconductors (UMS) foundry delivers a range of processes and services that bring value and benefit to clients. State-of-the-art systems, design kits, and scalable reliable models, support the design and production of high performance Gallium Arsenide MMICs.

In support of foundry services, training and mentoring is available from UMS’ highly experienced professionals, who have depth and breadth of experience in the design and application of GaAs technology in successful Defense, Aerospace, Telecoms and Industrial solutions.

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<th>Process</th>
<th>ADS Schematic</th>
<th>ADS Desktop DRC</th>
<th>ADS Layout</th>
<th>Momentum Substrate</th>
<th>MMIC Tool Bar</th>
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Complete MMIC/Module ADS Desktop Flow

**MMIC Overview**

The MMIC ADS Desktop Flow provides the industry's strongest, most complete set of MMIC design tools available in one environment:

- Integrated multi-solver electro-magnetic technology to help deal with the challenge of increasing complexity
- A foundry-endorsed design environment to help streamline the foundry-submission process
- Full manufacturing layout tightly integrated with schematic
- The convenience of a DRC and LVS tool on every MMIC designer’s desktop

### Design Capture

**Getting Started**
- Project Management
- Component Insertion
- MMIC Tutorial
- PDK Toolkit

**Foundry Submission**
- Artwork Formats
- Component Count
- Reticle
- Design Documentation

### Simulation

**Analysis**
- S-parameters
- Harmonic Balance
- Transient
- Envelope
- Tuning
- Optimization
- Design for Manufacturing
- Data Display

**Device Models**
- FET Models
- Bipolar Models
- User-Defined and Custom Models
- Model Extraction

### Layout

**Layout Editing**
- Artwork
- Interconnect
- Layers
- MMIC Toolbar

**Layout Verification**
- DRC
- LVS
- 3D Layout Preview
- Layout Connectivity Checker

### Physical Modeling

**3D Planar Analysis**
- Momentum
- Layout Components
- Advanced Model Composer

**Full 3D Analysis**
- FEM Simulator
- Layout Components
- Bond Wires and Dielectric Bricks

### MMIC Applications

- Low-Noise Amplifier
- Power Amplifier
- Wireless Verification
- Load Pull
- MMIC Examples

---

Additional Resources
- What's New
- Articles
- Knowledge Center
- Technical Support
- Training
- Videos

Related Links
- MMIC Design
- MMIC Seminar
- Foundry Partners

http://www.agilent.com/find/eesof-mmic-overview
MMIC Overview

• One-stop shop for information on all the MMIC capability available in ADS today

• Designed to help customers’ evaluations successful

• Topic pages contain
  – Value statements
  – Features
  – Tutorials
  – Examples
  – Links to user documentation
  – Videos
  – Graphical illustration

http://www.agilent.com/find/eesof-mmic-overview

Help>Getting Started with ADS…
Educational Material Available
MMIC Design Seminar Material

- Seminar Videos
- Presentations & Demos
- ADS projects
- Hands-on Workshops
- X-Parameters

http://www.agilent.com/find/eesof-mmic-seminar

Note: The MMIC Design Seminar videos, presentations, ADS projects, workshops and more (January 2009) have been compiled on an easy to use DVD for your convenience. Click here to Order the Agilent MMIC Design Seminar on DVD

Watch:
- Video Demos on Generating X-parameters* from Circuit Level Designs
- New Optimization Cockpit in ADS 2009 Update 1 Video Demo
- New "Easy to Use" Layout Tool Bar Video Demo

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<th>MMIC Design Seminar Materials</th>
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<td><strong>X-Parameters</strong></td>
<td>Agilent NVNA and X-Parameter Simulation in ADS</td>
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<tr>
<td>Front-to-Back MMIC Design</td>
<td>Our complete design flow for MMIC design with ADS</td>
</tr>
<tr>
<td>Layout</td>
<td>Discover the power of Advanced Design System (ADS) Layout</td>
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<tr>
<td>Trace and Via Insertion</td>
<td>Learn how easy it is to automatically insert traces and vias with the single push of a key</td>
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<tr>
<td>Design Rule Checker</td>
<td>View a demonstration of the ADS Design Rule Checker</td>
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<tr>
<td>Design for Manufacturing</td>
<td>Transform standard designs into robust ones with first-pass success and high yield</td>
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<tr>
<td>Design of Experiments</td>
<td>Learn methods to pinpoint the source of yield problems in a design</td>
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<tr>
<td>Yield Sensitivity Histograms</td>
<td>Gain valuable insight into your designs with Yield Sensitivity Histograms</td>
</tr>
<tr>
<td>Sensitivity Analysis</td>
<td>Compute any response versus any design variable - go beyond the traditional SPICE sensitivity analysis</td>
</tr>
<tr>
<td>Package and Bondwire Effects with EMDS</td>
<td>View a demonstration of how ADS is used to verify a MMIC Ku-band LNA using its integrated simulator</td>
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</tbody>
</table>

* "X-parameters" is a registered trademark of Agilent Technologies. The X-parameter format and underlying equations are open and documented. For more information
Thank you for your attention

Any question?

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- UMS USA: +1 978 905-3162
- UMS Asia: +8621 6103 1635

www.ums-gaas.com

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